

What is claimed is:

1. A method for determining a location of a mobile device, comprising:  
receiving a signal from a first base station;  
receiving a signal from a second base station;  
determining a location of the mobile device based on the received signals;  
and  
transmitting the location of the mobile device to a server.

Sub A/ 1. A method of reducing electrical power consumption by a digital computer when said computer is supplied with electrical power, but fails to process a computer application program for a prescribed period of inactivity, said digital computer, including a processor, said processor producing and maintaining an internal context, comprising the computer implemented steps of:

determining if said prescribed period of inactivity has been attained, and, in response to an affirmative determination;

preserving said internal context against loss due to removal of electrical power from said processor;

removing all electrical power from said processor, whereby said processor is powered down, notwithstanding continued supply of electrical power to said computer; and

restoring electrical power to said processor and restoring said preserved internal context to said processor when processing is to resume.

2. The method defined in claim 1, wherein said step of preserving said internal context against loss due to removal of electrical power from said processor, includes the steps of:

reading said internal context from the internal memory of said processor prior to removal of electrical power from said processor, said internal memory comprising internal registers; and

writing said internal context into a second memory, said second memory being electrically powered separately from said processor, wherein removal of electrical power from said processor leaves electrical power to said second memory unaffected

3. The method as defined in claim 1 wherein said internal memory of said processor includes a cache memory; and wherein said step of preserving said internal context, includes the steps:

supplying electrical power to said cache memory separately from said processor, wherein removal of electrical power from said processor leaves electrical power to said cache memory unaffected to prevent loss of said internal context on removal of electrical power from said processor.

4. The method as defined in claim 1, wherein the step of restoring electrical power to said processor and restoring said preserved internal context to said processor when processing is to resume, further comprises the steps of:

initializing said processor;

determining whether application of electrical power was due to a power on reset condition or a resume from a suspend to RAM condition; and

upon determining that electrical power commenced due to a resume from a suspend to RAM condition, then accessing and installing said preserved internal context to said processor.

5. The method as defined in claim 2, wherein said step of restoring electrical power to said processor and restoring said preserved internal context to said processor when processing is to resume, further comprises the steps of:

initializing said processor;

5 determining whether restoration of electrical power to said processor is  
6 due to a power on reset condition or a resume from a suspend to RAM  
7 condition; and

8 upon determining that electrical power commenced due to a resume from  
9 a suspend to RAM condition, then accessing said preserved internal context in  
10 said second memory and reading back said internal context into said internal  
11 registers for access by said processor, whereby the internal context of said  
12 processor is restored.

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6 a power supply for supplying power separately to said CPU and said first  
7 and second memory;

8 said power supply including:

9 a rechargeable battery;

10 first power circuit means for distributing electrical power to said CPU;

11 second power circuit means for distributing electrical power to at least  
12 said first memory and said second memory; and

13 an on-off switch for closing power from said battery to each of said first  
14 and second power circuit means, whereby said first and second power circuit  
means is enabled to deliver power;

15 first program routine means for detecting inactivity of application  
16 instruction processing of said CPU for a period of time, T<sub>max</sub>;

17 second program routine means for saving the entire internal context of  
18 said CPU in said second memory and for producing an STR signature in  
19 response to a positive detection of inactivity by said first program routine  
20 means;

21 third program routine means for terminating distribution of power by  
22 said first power circuit means following completion of said second program  
23 routine means, whereby power is removed from said CPU while said internal  
24 context of said CPU is preserved in said second memory.  
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1 8. The processor as defined in claim 7, further comprising:

2 a user operated input device for enabling user input to said application;

3 means for enabling said second power circuit means to distribute power  
4 to said CPU, responsive to operation of said user operated input device;

5 program means responsive to re-energization of said CPU for initiating an  
6 initialization process for said CPU;

7 loading and processing a boot loader;

8 configuring internal memory of said CPU, excluding said second memory;

9 reset registers of said CPU; and

10 checking for STR signature;

11 fourth routine program means, responsive to detection of said STR  
12 signature, for retrieving the portion of said internal context of said CPU earlier  
13 stored in said internal memory of said CPU and reading back said portion into  
14 the internal registers of said CPU, and retrieving said context of said  
15 Northbridge registers and loading said context in said internal memory of said  
16 CPU.

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9. The processor as defined in claim 8, further comprising:

2 fifth routine program means for retrieving the next instruction of the  
3 application program for execution by said CPU, responsive to completion of  
4 said fourth routine program means.

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10. A processing system, comprising:

2 a central processing unit for processing instructions, said central  
3 processing unit including internal registers;

4 a first memory;

5 a second memory;

6 Code morphing program means defining a virtual X86 processing system,  
7 said virtual X86 processing system including a virtual X86 central processing  
8 unit and a virtual Northbridge chip, whereby instructions of an X86 application  
9 program may be processed in said processing system;

10 a power supply for supplying power separately to said CPU and said first  
11 and second memory;

12 said power supply including:

13 a rechargeable battery;

14 first power circuit means for distributing electrical power to said CPU;

15 second power circuit means for distributing electrical power to at least  
16 said first and second memory; and

17 an on-off switch for closing power from said battery to each of said first  
18 and second power circuit means, whereby said first and second power circuit  
19 means is enabled to deliver power;

20 first program routine means for detecting inactivity of application  
21 instruction processing of said CPU for a period of  $T_{max}$ ;

22 second program routine means for saving the entire internal context of  
23 said CPU in said second memory and for producing an STR signature in  
24 response to a positive detection of inactivity by said first program routine  
25 means;

26 third program routine means for terminating distribution of power by  
27 said first power circuit means following completion of said second program  
28 routine means, whereby power is removed from said CPU and said CPU is

29 placed in an off state while said internal context of said CPU is preserved in  
30 said second memory.

31

1 11. The processor as defined in claim 10, further comprising:

2 means for enabling said second power circuit means to distribute power  
3 to said CPU, responsive to operation of said user operated input device;

4 program means responsive to re-energization of said CPU for initiating an  
5 initialization process for said CPU;

6 loading and processing a boot loader;

7 configuring internal memory of said CPU, excluding said second memory;

8 resetting the registers of said CPU; and

9 checking for an STR signature;

10 fourth program routine means, responsive to detection of said STR  
11 signature, for retrieving the portion of said internal context of said CPU earlier  
12 stored in one of said first and second memory and reading back said portion  
13 into the internal registers of said CPU, and retrieving said context of said  
14 Northbridge registers earlier stored in one of said first and second memory and  
15 loading said context in said internal registers of said CPU.

16

1 12. A digital computer comprising: a CPU; a private memory; and a power  
2 supply, said power supply for supplying power to said CPU and said private  
3 memory independent of one another to enable withdrawal of power from said  
4 CPU without withdrawal of power from said private memory; said CPU defining  
5 and maintaining a CPU context to enable processing of application programs;  
6 and said CPU context being stored in said private memory, whereby said



7 context is retained upon withdrawal of power from said CPU without  
8 withdrawal of power from said private memory.

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13 Sub A 13. The digital computer defined in claim 12, wherein said digital computer  
14 comprises a host computer for dynamically translating and executing  
15 instructions of a target application designed for processing by a target  
16 computer containing an instruction set different from the instruction set of the  
17 host computer.

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